20

```
Library ieee;
use ieee.std_logic_1164.all;

ENTITY mydesign IS
 PORT  (in1, in2:        in std_logic_vector(3 downto 0);
          out1, out2:    outstd_logic_vector(3 downto 0);
end;

ARCHITECTURE udcounter_arch of udcounter IS
signal sig1, sig2: std_logic_vector(3 downto 0);
begin
.
.
.
 sig1 <= in1 or in2
 sig2 <= in2 and in2;
 out1 <= FT(sig1); --Out1 is a critical function.  Implement 3 copies and voter in
 FPGA.
 out2 <= sig2; ==Out2 is not fault tolerant.  Create only one copy.
end
```

FIG. 1

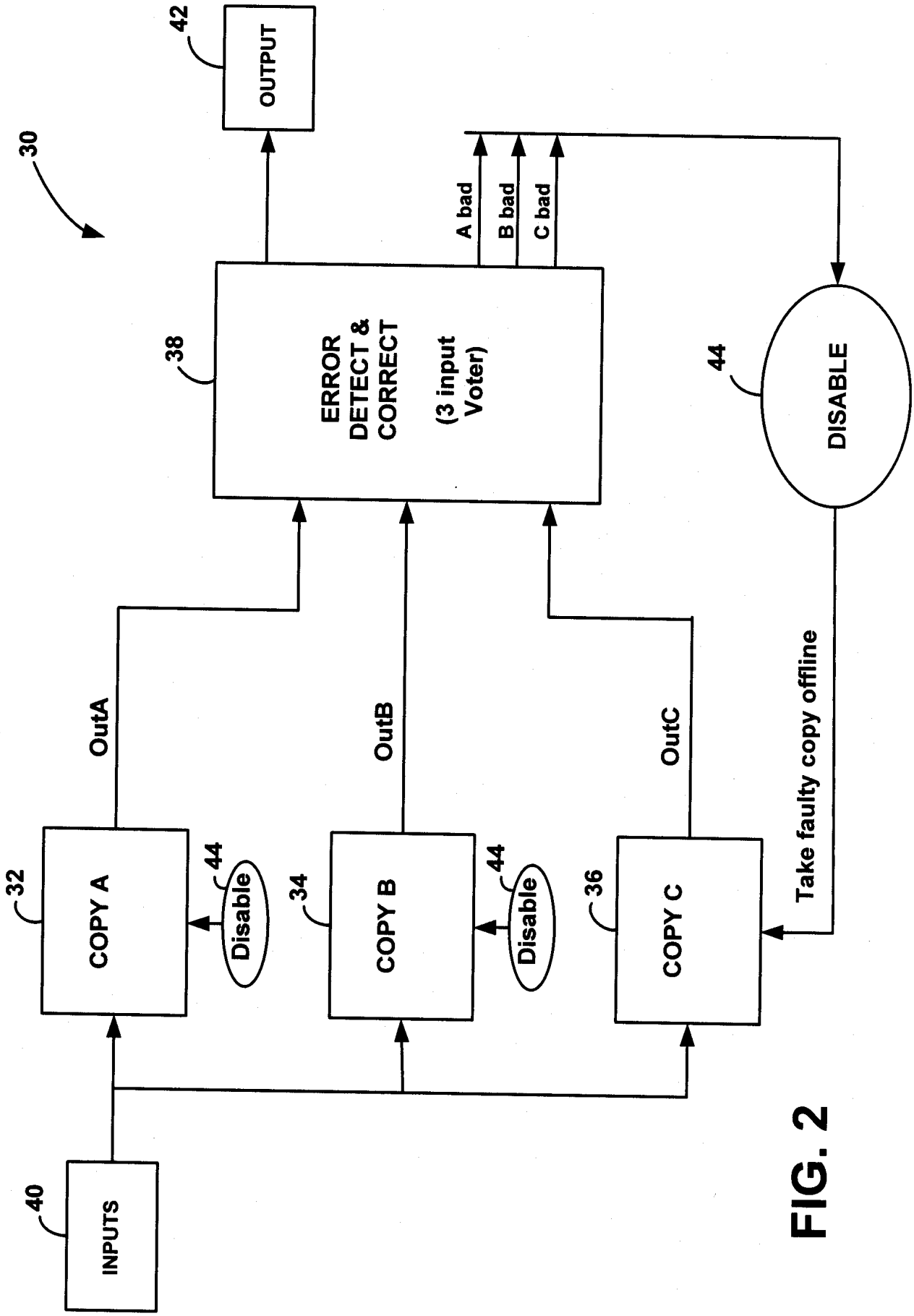
30
42
OUTPUT
A bad
B bad
C bad
38
ERROR DETECT & CORRECT (3 input Voter)
44
DISABLE
OutA
OutB
OutC
Take faulty copy offline
32
COPY A
44
Disable
34
COPY B
44
Disable
36
COPY C
40
INPUTS

FIG. 2